32-channel High Voltage Power Supply EHQ 20 025p

Operators Manual

Contents

Attention!

-The device must not be operated with the cover removed.

-We decline all responsibility for damages and injuries caused by an improper use of the module. It is highly recommended to read the manual before any kind of operation.

Note

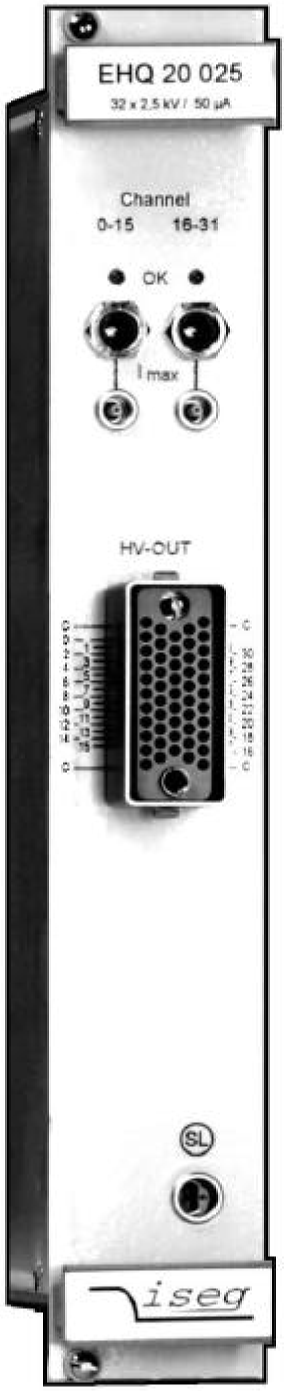
Filename EHQ20025p_V204eng.___; version 2.04 as of 2000-10-16

1. General information

The EHQ 20 025 is a 32-channel high voltage power supply in 6U Eurocard format. Each single channel is independently controllable. The EHQ 20 025 is made ready for mounting into a crate. The powered system crate ECH 228 (19“ rack) carries up to 8 modules. It is also possible to supply the modules separately with the necessary power. The unit is software controlled via CAN-Interface directly through a PC or similar controller.

2. Technical data

	EHQ 20 025p
Output current I_O	max. 50 µA
per channel at V_O	0 to + 2500 V
Ripple and noise	f = 10 Hz to 100 MHz: < 10 mV (at max. load) under two conditions: - at V_O > 400 V and - the different voltage between the channels must be less than 1000 V_O, e.g. $V_{O\,CH31} = 2500$ V $\Rightarrow V_{O\,CHn} \geq 1500$ V; (n= 0 to 30)
Current limit I_{max}	Potentiometer (I_{max} is the same for 16 channels)
Interface	CAN-Interface
Voltage setting	via software, resolution 50 mV
Voltage measurement	via software, resolution 50 mV
Current measurement	via software, resolution 2 nA
Accuracy of voltage measurement	$\pm$ (0,01% $*$ V_O + 0,02% $*$ $V_{O\,max}$ + 1 digit) for one year
Accuracy of current measurement	$\pm$ (0,1% $*$ I_O + 0,4% $*$ $I_{O\,max}$ + 1 digit) for one year
Temperature coefficient	$< 5 * 10^{-5}/_K$
Stability	$< 5 * 10^{-5}$ (no load/load and Δ V_{IN})
Rate of change of output voltage via softw.	1 V/s to 125 V/s resolution 0,5 V/s 125 V/s to 250 V/s resolution 5 V/s
Channel control via software	Status 8 bit: voltage and current limit, KILL-enable, channel emergency cut-off, ramp, channel on/off, input error, current trip
16 Channels error control via software	voltage limit current limit (″16 Channels OK″ is signalled if these limits do not exceed on each.)
Error signal	Green LED at ″16 Channels OK″
Protection loop (I_s) (2 pin Lemo-socket)	5 mA < I_s < 20 mA $\Rightarrow$ module on I_s < 0,5 mA $\Rightarrow$ module off
Power requirements V_{IN}	+ 24 V (<1 A) and + 5 V (< 1,3 A)
Packing	32-channels in 6U Euro cassette (40,64 mm wide and 220 mm deep)
Connector	96-pin connector according to DIN 41612
HV connector	51-pin Redel Multipin-Connector



3. Handling

The supply voltages and the CAN interface is connected to the module via a 96-pin connector on the rear side of the module.
The maximum output current for the channels 0 to15 and 16 to 32 are defined through the position of the corresponding potentiometer I_{max} .
It is possible to measure the hardware current limit, which has been set with reference to the maximum possible current at the socket below. 100 % I_{max} corresponds to 2,5 V. The output current will be limited to the setting value after it exceeds the threshold and the corresponding green LED on the front panel is ‘OFF‘.
At the bottom on the right side of the front panel is the socket for the safety loop. If the safety loop is active then output voltage is only present if a current is flowing in a range of 5 to 20 mA of any polarity (i.e. safety loop closed). If the safety loop is opened during operation then the output voltages are shut off without ramp and the corresponding bit in the ‘Status module’ will be cancelled. After the loop will be closed again the channels must be switched ‘ON’ and a new set voltage must be given before it is able to offer an output voltage. The pins of the loop are potential free, the internal voltage drop is ca. 3 V. Coming from the factory the safety loop is not active (the corresponding bit is always set). Removing of an internal jumper makes the loop active.
(s. App. A).

Pin assignment 96-pin connector according to DIN 41612:

PIN		PIN		PIN		Data
a1 a3 a5		b1 b3 b5		c1 c3 c5		+5V +24V GND
a11		b11		c11		@CAN_GND @CANL } potential free @CANH
a13						RESET
a30 a31 a32	A4 A2 A0	b30 b31 b32	A5 A3 A1	c30 c31 c32	GND GND GND	} Address field module address (A0 ... A5)

With the address field a30/b30 ..... a32/b32 the module address will be coded.
(see item 4.4, description 11bit-Identifier).
Connected to GND ⇒ A(n) = 0 ; contact open ⇒ A(n) = 1

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4. Communication via interface

4.1 Device Control Protocol DCP

The communication between the controller and the module works according to the Device Control Protocol DCP, which has been designed for the use of multi-level-hierarchy systems for instruments.

This protocol works according to the master slave principle. Therefore, the controllers who are on higher hierarchy always are masters while devices, which are in lower hierarchy, work as slaves.

In the event of the control of the HV device through a controller the controller will have the master function in this system, while the module (as a Front-end device with intelligence) will be the slave.

The data exchange between the controller and the Front-end (FE) device works with help of data frames. These data frames are assembled of one direction bit DATA_DIR, one identifier bit DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame is a write or read-write access. The DATA_ID carries the information of the type of the data frame and occasionally sub addresses (G0, G1). It is characterised through the first byte of the data frame with bit 7=1. The function of the module as part of a complex system will be defined through the DATA_ID .

In such systems with many hierarchical levels a single function of a single module can be addressed by using group controllers (GC). Then, for each GC on the way to the module the data frame is crated through nesting of the address fields of the GC-addresses followed by the DATA_ID (not necessary in case of control a single module).

EXT_ INSTR	DATA _DIR	DATA_ID Bit								Access
		7	6	5	4	3	2	1	0	
	x	**0**	x	x	x	x	x	x	x	**No** DATA_ID
0/1	**0**	1	0	x	x	x	x	x	x	**Write access** on Front-end device
0/1	**1**	1	0	x	x	x	x	x	x	**Read-write access** on Front-end device (Request at Write)
0/1	**0**	1	1	x	x	x	x	**G1**	**G0**	**Write access** on group
0/1	**1**	1	1	x	x	x	x	**G1**	**G0**	**Read-write access** on group (Request at Write)
										G0, G1 sub address Only needed if group controller (GC) is used

These data frames correspond to a transfer into layer 3 (Network Layer) respectively layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is CAN Bus according to specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

The Device Control Protocol DCP has been matched to the CAN Bus according to specification CAN 2.0A, but it is also possible to be matched to further transmission media (e.g. RS232). Therefore specials of layer 1 and 2 are only mentioned if absolutely necessary and if misunderstandings of functions between the Transport Layer and functions of the Data Link Layer may be possible. The communication between the controller and a module on the same bus segment will be described as follows.

4.2 Summary of CAN data frames

The 32-channel Module EHQ 20 xxx is added at two 16-channel modules, which are controlled independently of each other.

Following list describes the accesses of the DCP made for one 16-channel module.

EXT_ INSTR	DATA_ DIR	DATA_ID Bit								Access	read/ write/ active	DATA - Bytes
ID1	ID0	7	6	5	4	3	2	1	0			
	x	**0**	x	x	x	x	x	x	x	**No DATA_ID**		
x	**x**	**1**	**0**	**C1**	**C0**	**N3**	**N2**	**N1**	**N0**	**Single access CHANNEL:**		
1	1/0	1	0	0	0	N3	N2	N1	N0	Current trip	r/w	3
0	1	1	0	0	0	N3	N2	N1	N0	Actual voltage	r	3
0	1	1	0	0	1	N3	N2	N1	N0	Actual current	r	3
0	1/0	1	0	1	0	N3	N2	N1	N0	Set voltage	r/w	3
0	1	1	0	1	1	N3	N2	N1	N0	Status channel	r	3
x	**x**	**1**	**1**	**C3**	**C2**	**C1**	**C0**	**G1**	**G0**	**Group access module**		
1	1	1	1	0	0	0	0	0	0	Voltage supplies and module temperature	r	8
0	1/0	1	1	0	0	0	0	0	0	General status module	r/w a	2
0	1	1	1	0	0	0	1	0	0	Status1 Voltage limit was exceeded at single channel	r	3
0	1	1	1	0	0	1	0	0	0	Status2 Hardware current limit was exceeded at single channel	r	3
0	1/0	1	1	0	0	1	1	0	0	Channel ON / OFF	r/w	3
0	1/0	1	1	0	1	0	0	0	0	Ramp speed	r/w	3
0	0	1	1	0	1	0	1	0	0	Emergency cut-out	w	3
0	1	1	1	0	1	1	0	0	0	Log-on Front-end device in superior layer	a	2
0	0	1	1	0	1	1	0	0	0	Log-off superior layer at Front-end device	w	2
0	1/0	1	1	0	1	1	1	0	0	Bit rate	r/w	3
0	1/0	1	1	1	0	0	0	0	0	Serial number, software release and CAN message configuration	r/w	6/2
0	0	1	1	1	0	0	1	0	0	Set voltage for all channels	w	3
0	1	1	1	1	0	1	0	0	0	Read hardware current limit	r	3
0	1/0	1	1	1	0	1	1	0	0	KILL-enable	r/w	3
0	1/0	1	1	1	1	0	0	0	0	ADC filter setting	r/w	3
0	1	1	1	1	1	0	1	0	0	Module nominal values	r	5
0	1	1	1	1	1	1	0	0	0	Status3 Software current trip was exceeded at single channel	r	3
		C_i:				Accesses						
		N_i		0 to 15:		Channel 0 to 15						
		G_i:		0 to 3:		Group 0 to 3 Only needed if group controller (GC) used						

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4.3 Detailed CAN data frames description

Log-on and Log-off Front-end (FE) device (active/write access)

Log-on frame 16-channel **module** (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7		5	4	3	2	1	0
Designation	DATA _DIR							G1	G0								
Data	1	1	1	0	1	1	0	0	0			u	v	w	x	y	z
Description	active	G1 to G0: Group 0 to 3 Only needed if group controller (GC) is used								Values of bit z to u: see **Group access: General status module**							

After POWER ON the module will give this group access cyclically on the bus (ca. 2...10 sec).

Bit 0 to 5 in DATA_0 describes the general status of the module (see **Group access: General status module)**. If a controller identifies this access then it is able to register this module as a Front-end device and is able to address it with FE_ADR.

The 16-channel module with the hardware channels 0 to 15 will send an even FE_ADR and the 16-channel module with the hardware channels 16 to 31 an uneven FE_ADR.

(Module address, see also item 4.4, description 11bit-Identifier)

Remote-frame **Log-on controller** (DLC = 2)

Byte		DATA_ID								DATA_0	
Bit		7	6	5	4	3	2	1	0		0
Designation	DATA_DIR							G1	G0		
Data	0	1	1	0	1	1	0	0	0		1
Description	write	G1 to G0: Group 0 to 3 Only needed if group controller (GC) is used								Module is log-on	

The module will not send further ‘Log-on controller’ accesses after the successful registration as long as it receives accesses from the external CAN Bus in periods shorter than one minute respectively until the controller will send a ‘Log-off controller” access to the Front-end device.

Remote-frame **Log-off controller** (DLC = 2)

Byte		DATA_ID								DATA_0	
Bit		7	6	5	4	3	2	1	0		0
Designation	DATA_DIR							G1	G0		
Data	0	1	1	0	1	1	0	0	0		0
Description	write	G1 to G0: Group 0 to 3 Only needed if group controller (GC) is used								Module is log-off	

Single access CHANNEL: Current trip (Read-write/Write access), **extended access list**

Read-write

Byte	Identifier		DATA_ID							
Bit	ID1	ID0	7	6	5	4	3	2	1	0
Designation	EXT_ INSTR	DATA _DIR					N3	N2	N1	N0
Data	1	1	1	0	0	0	x	x	x	x
Description		read	Channel N_x off 0 ... 15							

Controller (DLC = 1):
Read actual software current trip
at the corresponding channel

⇓ Response module (DLC = 3)

Byte	Identifier		DATA_ID								DATA_1			DATA_0		
Bit	ID1	ID0	7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	EXT_ INSTR	DATA _DIR					N3	N2	N1	N0						LSB
Data	1	0	1	0	0	0	x	x	x	x	x					
Description		write	Channel N_x off 0 ... 15								Actual current trip with resolution $I_{O\ max}$ / 25000 [A] in DATA_1 and DATA_0					

Write (Controller [DLC = 3]: Write software current trip at corresponding channel)

Byte	Identifier		DATA_ID								DATA_1			DATA_0		
Bit	ID1	ID0	7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	EXT_ INSTR	DATA _DIR					N3	N2	N1	N0						LSB
Data	1	0	1	0	0	0	x	x	x	x	x					
Description		write	Channel N_x off 0 ... 15								Actual current trip with resolution $I_{O\ max}$ / 25000 [A] in DATA_1 and DATA_0					

If the channel is in 'ON' and the measured output current will exceed the programmed current trip, then the voltage will be shut off without ramp (Bit o = 0 in 'Status channel').

At the same time bit t in 'Status channel' and bit z in ' General status module' will be set. These bits will be resets if 'Status3 Software current trip' will be read.

With help of the 'Group access' 'Switch **ON** /OFF' the concerning channels are switched ON again.

Function will be switched off with write 'Current trip = 0'.

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Single access CHANNEL: Actual voltage (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR					N3	N2	N1	N0
Data	1	1	0	0	0	x	x	x	x
Description	read	Channel N_x of 0 ... 15							

Controller (DLC = 1):
Read actual voltage at the corresponding channel

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR					N3	N2	N1	N0						LSB
Data	0	1	0	0	0	x	x	x	x	x					
Description	write	Channel N_x of 0 ... 15								Actual voltage with resolution $V_{O\,max}$ / 50000 [V] in DATA_1 and DATA_0					

Single access CHANNEL: Actual current (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR					N3	N2	N1	N0
Data	1	1	0	0	1	x	x	x	x
Description	read	Channel N_x of 0 ... 15							

Controller (DLC = 1):
Read actual current at the corresponding channel

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	..	0	7	..	0
Designation	DATA_DIR					N3	N2	N1	N0						LSB
Data	0	1	0	0	1	x	x	x	x	x					
Description	write	Channel N_x of 0 ... 15								Actual current with resolution $I_{O\,max}$ / 25000 [A] in DATA_1 and DATA_0					

Single access CHANNEL: Set voltage (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR					N3	N2	N1	N0
Data	1	1	0	1	0	x	x	x	x
Description	read	Channel N_x of 0 ... 15							

Controller (DLC = 1):
Read set voltage at the corresponding channel

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR					N3	N2	N1	N0						LSB
Data	0	1	0	1	0	x	x	x	x		x				
Description	write	Channel N_x of 0 ... 15								Set voltage with resolution $V_{O\,max}$ / 50000 [V] in DATA_1 and DATA_0					

Write (Controller [DLC = 3]: Write set voltage at corresponding channel)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR					N3	N2	N1	N0						LSB
Data	0	1	0	1	0	x	x	x	x	x					
Description	write	Channel N_x of 0 ... 15								Set voltage with resolution $V_{O\,max}$ / 50000 [V] in DATA_1 and DATA_0					

If the channel is switched ‘ON’ then the voltage will be ramped to the set value after the receipt of this access. Otherwise the set value will just be stored and only used for ramping to the set voltage after the channel will be switched ‘ON’.

Set voltages higher than the maximum module voltage will be ignored and the bit ‘Input error’ of the ‘Status channel’ will be set.

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Single access CHANNEL: Status channel (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR					N3	N2	N1	N0
Data	1	1	0	1	1	x	x	x	x
Description	read	Channel N_x of 0 ... 15							

Controller (DLC = 1):
Read channel status at the corresponding channel

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1								DATA_0	
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7 ... 1	0
Designation	DATA_DIR					N3	N2	N1	N0	v	c	k	n	r	o	i	f		t
Data	0	1	0	1	1	x	x	x	x	x	x	x	x	x	x	x	0		x
Description	write	Channel N_x of 0 ... 15																	

Input-error
i=0, no input-error
i=1, set voltage, f_N or ramp out off set range

o=0 ⇒ Channel OFF
o=1 ⇒ Channel ON

Voltage state
r=0 ⇒ Voltage is stable
r=1 ⇒ Voltage ramps

Channel Emergency cut-off
n=0 ⇒ Channel works
n=1 ⇒ Cut-off (only to first write in DAC)

KILL-enable
k=0 ⇒ KILL function disable: V_O shut off if current limit was exceeded and then V_O is ramping from 0V to V_{SET}
k=1 ⇒ KILL function enable: V_O shut off permanently if current limit was exceeded

Current limit
c=0 ⇒ Channel is ok
c=1⇒ V_O shut of 0 V because hardware current limit was exceeded

Voltage limit
v=0 ⇒ Channel is ok
v=1 ⇒ V_O shut of permanently because voltage limit was exceeded

Current trip
t=1 ⇒ V_O shut of 0 V because software current trip was exceeded

Group access: Voltage supplies and module temperature (Read-write), **extended access list**

Read-write

Byte		Identifier			DATA_ID							
Bit		ID1	ID0		7	6	5	4	3	2	1	0
Designation		EXT_ INSTR	DATA _DIR									
Data		1	1		1	1	0	0	0	0	0	0
Description			read									

Controller (DLC = 1):
Read voltage supplies and the module temperature

⇓ Response module (DLC = 8)

Byte		Identifier			DATA_ID								DATA_n						
Bit		ID1	ID0		7	6	5	4	3	2	1	0	6	5	4	3	2	1	0
Designation		EXT_ INSTR	DATA _DIR										U1	U2	U3	U4	U5	t2	t1
Data		1	0		1	1	0	0	0	0	0	0	x	x	x	x	x	x	x
Description			write										+24V	+15V	+5V	-15V	-5V	Temperature	
													U1 to U5: Voltage resolution 100 mV						
													t2 & t1: Module temperature resolution 0,1 °C						

Out of range (see **Group access: General status module**) will be generated at tolerance of voltage supplies are greater then ± 5%.

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Group access: General status module (Read-write/Write/Active access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	0	0	0	0
Description	read								

Controller (DLC = 1):
Read status at the corresponding module

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7		5	4	3	2	1	0
Designation	DATA_DIR																
Data	0	1	1	0	0	0	0	0	0			u	v	w	x	y	z
Description	write									z=1 'Status channel' bit c & v & t = 0 for all channels: no current limit/trips and no voltage limit were exceeded in the module z=0 current limit/trips or voltage limit were exceeded at least one channel y=1 no channel is ramping y=0 V_O is ramping at least one channel x=1 safety loop is closed x=0 V_O was shut off with safety loop, if safety loop is closed again the bit would set at first read w=1 V_O is ramping at least one channel with ADC filter frequency f_N = 100 Hz w=0 all channels are stable with programmable ADC filter frequency f_N (ADC conversion time = 1 / f_N , see 'ADC filter frequency setting', ex works f_N = 50 Hz) v=1 fine adjustment ON v=0 fine adjustment OFF u=1 voltage supplies in range u=0 voltage supplies out of range							

Write (Controller [DLC = 2]: Write fine adjustment ON / OFF)

Byte		DATA_ID								DATA_0				
Bit		7	6	5	4	3	2	1	0	7	...	4	...	0
Designation	DATA_DIR													
Data	0	1	1	0	0	0	0	0	0	masked		v	masked	
Description	write									v=1 fine adjustment ON v=0 fine adjustment OFF				

If the fine adjustment 'ON' then the ADC filter will working with the programmable f_N after ramping to the set voltage.

If the fine adjustment 'OFF' then the ADC filter works with f_N=100 Hz.

f_N ... filter first notch frequency

Active (Module [DLC = 2]: Module sends total error **active** with high priority, reaction time < 150 ms)

Byte	Identifier		DATA_ID								DATA_0							
Bit			7	6	5	4	3	2	1	0	7		5	4	3	2	1	0
Designation	ID9	DATA _DIR																
Data	0	1	1	1	0	0	0	0	0	0			**u**	v	w	**x**	y	**z**
Description		active									If u & x & z = 0, then the module send once active this error frame with ID9 = 0							

The module was configured as a CAN-node with an Active-CAN message function (see **Group access: Serial number, software release and CAN message configuration**). In this case the module will send this group access as an active error message with higher priority (ID9 = 0) than normal messages are sent, if one of the sumstatus- and safety loop-bits in the group access “General status module” has not been set.

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Group access: Status1 Voltage limit (Read-write access)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	0	1	0	0
Description	read								

Controller:
Check exceeding voltage limit per channel

⇓ Response module (DLC = 3)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0	DATA_1 7	...	0	DATA_0 7	...	0
Designation	DATA_DIR														
Data	0	1	1	0	0	0	1	0	0	x15	...	x8	x7	...	x0
Description	write									x0 ⇒ Status for Channel 0 : x15 ⇒ Status for Channel 15			x_n = 0 ⇒ Channel ok x_n = 1 ⇒ Voltage limit was exceeded		

If an external over voltage occurs at the channel output (i.e. Output voltage > Set voltage) then the channel will be switched off and the according bit will be set. Only after the read of 'Status 1 voltage limit' this bit will be cancelled.

Group access: Status2 Hardware current limit (Read-write access)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	0	1	0	0	0
Description	read								

Controller (DLC = 1):
Check exceeding hardware current limit per channel

⇓ Response module (DLC = 3)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0	DATA_1 7	...	0	DATA_0 7	...	0
Designation	DATA_DIR														
Data	0	1	1	0	0	1	0	0	0	x15	...	x8	x7	...	x0
Description	write									x0 ⇒ Status for Channel 0 : x15 ⇒ Status for Channel 15			x_n = 0 ⇒ Channel ok x_n = 1 ⇒ Hardware current limit has been exceeded.		

The module responds to the exceeding of the hardware current limit which has been set in the channel in dependence to the according KILL-enable bit (see also Group access 'KILL-enable') as follows:

KILL-enable = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off.
KILL-enable = 0: Voltage will be switched off without ramp, green LED on front panel is off. If the output voltage arrives at 0 V ramping to set voltage will be started automatically again.
The green LED only flash on again after read the Group access 'Status2 Hardware current limit'.

Group access: Channel ON / OFF (Read-write /Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR								
Data	1	1	1	0	0	1	1	0	0
Description	read								

Controller (DLC = 1):
Check Channels ON or OFF

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	...						0	7							0
Designation	DATA _DIR																								
Data	0	1	1	0	0	1	1	0	0	x15	...						x8	x7	...						x0
Description	write									x0 ⇒ Bit for Channel 0 $x_n = 1$ ⇒ Channel ON : x15 ⇒ Bit for Channel 15 $x_n = 0$ ⇒ Channel OFF															

Write (Controller [DLC = 3]: Channels shut ON or OFF define)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	...						0	7	...						0
Designation	DATA _DIR																								
Data	0	1	1	0	0	1	1	0	0	x15							x8	x7							x0
Description	write									x0 ⇒ Bit for Channel 0 $x_n = 1$ ⇒ Channel ON : x15 ⇒ Bit for Channel 15 $x_n = 0$ ⇒ Channel OFF															

Group access: Emergency cut-off (Write access)

Controller (DLC = 3): Channels ‘Emergency cut-off’

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	...						0	7	...						0
Designation	DATA _DIR																								
Data	0	1	1	0	1	0	1	0	0	x15							x8	x7							x0
Description	write									x15 ... x0: for $x_n = 1$: Channel 15 ... Channel 0 Channels cut-off without ramp															

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Group access: Ramp speed (Read-write /Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	1	0	0	0	0
Description	read								

Controller (DLC = 1):
Read actual ramp speed of module

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7		0
Designation	DATA_DIR														
Data	0	1	1	0	1	0	0	0	0		...	x8	x7	...	x0
Description	write									x8 ... x0: Ramp speed of module with resolution $V_{O\ max}$ / 50000s					

Write (Controller [DLC = 3]: Write ramp speed module)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7		0
Designation	DATA_DIR														
Data	0	1	1	0	1	0	0	0	0		...	x8	x7	...	x0
Description	write									x8 ... x0: Ramp speed of module with resolution $V_{O\ max}$ / 50000s Ramp speed range: $V_{O\ max}$ / 2500s ≤ Ramp speed ≤ $V_{O\ max}$ / 10s)[1] Ramp speed higher than the maximum module specific ramp speed will be ignored and the Bit ‘ Input error’ in the ‘Status channel’ will be set.					

)[1] : sub values are rounded down to the next lower value, according to the resolution.

Group access: Set voltage for all channels (Write access)

Controller (DLC = 3): Set voltage for all channels

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR														LSB
Data	0	1	1	1	0	0	1	0	0						
Description	write									Set voltage for all channels with resolution $V_{O\ max}$ / 50000 [V] in DATA_1 and DATA_0					

If anyone channel is ‘ON’ then the voltage of which will be ramped on set voltage after the receipt of this write access.
If anyone channel is ‘OFF’ then the set voltage of which will be stored in the module and after the channel will be switched ‘ON’ ramping will be started up to the set voltage.

Set voltages higher than the maximum specific module voltage will be ignored and the Bit ‘Input Error’ in ‘Status channel’ will be set.

Group access: Bit rate (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	0	1	1	1	0	0
Description	read								

Controller (DLC = 1):
Read actual bit rate

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7			...				0	7							0
Designation	DATA_DIR																								
Data	0	1	1	0	1	1	1	0	0				...				x8	x7			...				x0
Description	write									x8 ... x0: actual bit rate [kbit/s]															

Write (Controller [DLC = 3]: Write a new bit rate)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA_DIR																								LSB
Data	0	1	1	0	1	1	1	0	0								x8	x7	x6	x5	x4	x3	x2	x1	x0
Description	write									x8 ... x0: - 7 Bit rates are possible: 1) 20 kbit/s 2) 50 kbit/s 3) 100 kbit/s 4) 125 kbit/s 5) 250 kbit/s 6) (500 kbit/s on request) 7) (1000 kbit/s on request) - the new bit rate takes effect after RESET respectively POWER OFF/ON and - it has to be sure that the bit rate of all modules in the system must be the same before a RESET or POWER/ON is made. - bit rate is prefixed from factory signed on a sticker of the 96 pin connector. - invalid bit rates will be ignored from the module and the bit ‘Input error’ of the ‘Status channel 0’ will be set.															

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Group access: Serial number, software release and CAN message configuration

(Read-write/ Write access)

Read-write

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	0	0	0	0	0
Description	read								

Controller (DLC = 1):
Read serial number and software release module

⇓ Response module (DLC = 6)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0	DATA_4 BCD	BCD	DATA_3 BCD	BCD	DATA_2 BCD	BCD	DATA_1 BCD	BCD	DATA_0 BCD	BCD
Designation	DATA_DIR																		
Data	0	1	1	1	0	0	0	0	0	z6	z5	z4	z3	z2	z1	p1	y3	y2	y1
Description	write									6 BCD Serial number							3 BCD Software release		

Write (Controller [DLC = 2]: Write a new CAN message configuration)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0	DATA_0 BCD	BCD
Designation	DATA_DIR										
Data	0	1	1	1	0	0	0	0	0	0	x
Description	write									x = 2: with iseg Standard-CAN message ID9 is always dominant x = 4: with iseg Active-CAN message ID9 is recessive	

Group access: ADC filter frequency setting (Read-write/Write access)

(Programmable ADC conversion time = 1 / f_N , f_N ... filter first notch frequency)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR								
Data	1	1	1	1	1	0	0	0	0
Description	read								

Controller (DLC = 1):

Read actual ADC filter frequency f_N

- If all channels are stable this ADC filter frequency f_N is effective
- If V_O is ramping at least one channel then the ADC filter frequency is f_N = 100 Hz

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7		0
Designation	DATA _DIR														
Data	0	1	1	1	1	0	0	0	0	x15		x8	x7	...	x0
Description	write									ADC filter frequency f_N = 19200 / (x15 ... x0) [Hz]					

Write (Controller [DLC = 3]: Write new ADC filter frequency f_N)

Byte		DATA_ID								DATA_1		DATA_0							
Bit		7	6	5	4	3	2	1	0	7	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR																		LSB
Data	0	1	1	1	1	0	0	0	0	x15	x8	x7							x0
Description	write									(x15 ... x0) = 19200 / ADC filter frequency f_N [Hz] with 5 Hz ≤ f_N ≤ 100 Hz (invalid f_N will be ignored and the bit 'Input-error' in 'Status channel' is set). - if all channels arrive at V_{set} the first time, further measurements are made with this filter frequency. I.e.: V_{set} will be compared to V_{actual} averaging according to f_N - factory setting: f_N = 50 Hz									

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Group access: Read hardware current limit (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	0	1	0	0	0
Description	read								

Controller (DLC = 1):
Read hardware current limit setting with potentiometer

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7		0	7	..	0
Designation	DATA_DIR														LSB
Data	0	1	1	1	0	1	0	0	0	x					
Description	write									Hardware current limit with resolution $I_{O\ max}$ / 25000 [A] in DATA_1 and DATA_0					

Group access: KILL-enable (Read-write /Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	0	1	1	0	0
Description	read								

Controller (DLC = 1):
Read setting KILL function

KILL - enable: V_O shut off permanently
if hardware current limit was exceeded

KILL - disable: V_O shut off if current limit was exceeded
and then V_O is ramping from 0 V to V_{SET} again

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7		0
Designation	DATA_DIR														
Data	0	1	1	1	0	1	1	0	0	x15	...	x8	x7	...	x0
Description	write									x0 ⇒ Bit for Channel 0 x_n = 1 ⇒ KILL - enable : x15 ⇒ Bit for Channel 15 x_n = 0 ⇒ KILL - disable					

Write (Controller [DLC = 3]: Set KILL function)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR														
Data	0	1	1	1	0	1	1	0	0	x15		x8	x7		x0
Description	write									x0 ⇒ Bit for Channel 0 x_n = 1 ⇒ KILL - enable : x15 ⇒ Bit for Channel 15 x_n = 0 ⇒ KILL - disable					

Group access: Module nominal values (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	1	0	1	0	0
Description	read								

Controller (DLC = 1):
Read Voltage and Current nominal values of the module

⇓ Response module (DLC = 5)

Byte		DATA_ID								DATA_3			DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0	7	...	0
Designation	DATA_DIR																				
Data	0	1	1	1	1	0	1	0	0	x	...	x	x	...	x	x	...	x	x	...	x
Description	write									Mantissa V_{max}			Exponent V_{max}			Mantissa I_{max}			Exponent I_{max}		

Group access: Status3 Current limit (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	1	1	0	0	0
Description	read								

Controller (DLC = 1):
Check if the output current the software current trip per channel exceeds

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA_DIR														
Data	0	1	1	1	1	1	0	0	0	x15	...	x8	x7	...	x0
Description	write									x0 ⇒ Status for Channel 0 : x15 ⇒ Status for Channel 15			x_n = 0 ⇒ Channel ok x_n = 1 ⇒ Output current was exceeding the programmable current trip.		

If the measured output current exceeds the programmed current trip then the corresponding bits will be set. The output voltage is not present and the channel is ‘OFF’ (Bit o = 0 in ‘Status channel’). A programmed current limit with value zero has no effect to the current flow.

The setting bits in DATA_1 and DATA_0, the bit t in ‘Status channel’ and the bit z in ‘General status module’ will be resets after this access.

With help of the ‘Group access’ ‘Switch **ON** /OFF’ the concerning channels are switched ‘ON’ again.

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4.4 Implementation in the CAN-Bus

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0A, whereas looking from the point of view of the CAN protocol a pure data transmission will be done, which is not applying to the protocol.

The data frame of the DCP will be transferred as data-word with n bytes length in the data field of the CAN frames according to the specific demands of the respective access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.

It is possible to transfer 8 data bytes that apply to the DLC field with falling values.

The RTR Bit is always set to zero.

The information for the direction of the data transfer (DATA_DIR) is written in the lowest bit ID0 of the 11 Bit CAN-Identifier.

The controller therefore will start a read-write access for data with DATA_DIR = 1 and will send with DATA_DIR = 0.

The Front-end device responds to the data request with sending the corresponding data with DATA_DIR = 0.

Only if the Front-end device is not registered at the controller respectively if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA_DIR = 1 (see also item 4.3)

Therefore it follows that all even CAN-ports (Identifier) are interpreted as ‘Write ports’ all odd CAN ports as ‘ Read ports’.

The addressing of the Front-end device is also made with the 11 bit identifier of the CAN protocol.

In order to keep the CAN segment open also for other protocols, the addressing room was limited to 64 nodes.

ID10 is dominant.

ID9 - is always dominant for module’s witches have not an Active-CAN message function.

- is recessive for module’s witch have an Active-CAN message function when receive or send write- or read- write-accesses and is dominant when the module active send a error message.

If the module was configured as a CAN-node with an Active-CAN message function and the sumstatus-, safety loop- and voltage supplies-bit in the group access “General status module” are setting then the module send this group access us an active error message with higher priority (ID9 = 0) then normal messages are send.

ID3 to ID8 allow the addressing of 64 Front-end devices (ID3: A0 = 2^0 ;...; ID8: A5 = 2^5),

ID2 is not used.

In one CAN segment only modules are allowed with unequal identifier and equal bit rates. The factory fixed bit rate is written on the sticker of the 96-pin connector.

Following data frame is valid for the control of the Front-end device in this lowest CAN segment.

SOF	Identifier	RTR	0	0	DLC	n – data bytes				CRC	ack F.
					(n = 1 - 8)	DATA_ID	DATA_(n-2) ≥ 0	DATA_(n-3) ≥ 0	DATA_ ...		
	b10 b0		Reserv		b3 b0	b7=1 b0	b7 b0	b7 b0	b7 b0	15 bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	P	A5	A4	A3	A2	A1	A0		EXT_IN STR	DATA_DIR

Acceptance-Filter of the used CAN-Controller is set to Front-end-address

The Front-end device must do:

- Processing of the single accesses with direct channel values.
- Processing of group information of the channels.
- Self-registration in the higher level through sending the module address.
- Building of status information.
- Send an active error message with higher priority if one of the sumstatus- and safety loop -bits in the group access “General status module” has not been set (the module must be configured as a CAN-node with an Active-CAN message function).

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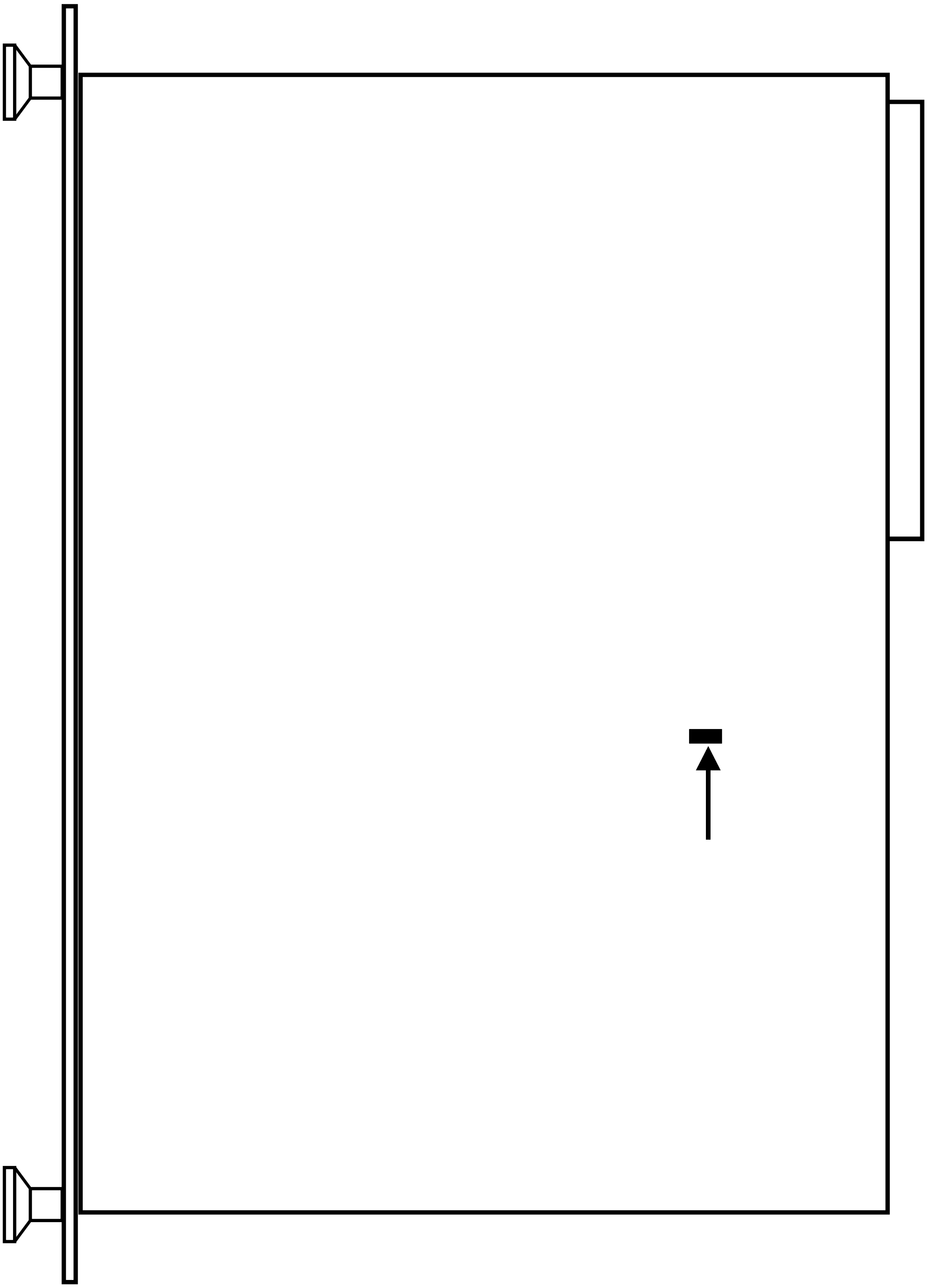

Appendix A: Side view

Desk open, jumper for safety-loop